Charge Pump Design for Use in NVM Device Test and Measurement

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Abstract. *Today, the emerging technology to fabricate deep-submicron Non-Volatile Memories (NVMs) requires extensive use of efficient methods for measurement and test. A high-voltage (HV) generator must be used to invoke NVM test modes, either placed on-chip or used from external. Our article focuses on the development of the Charge pump, being a core of such high-voltage generator. We consider an on-chip variant for the purpose of NVM measurement and test, the HV generator has to meet several criteria listed above. In our article we will particularly take into account the design criteria for the Charge pump to be used in such HV generator and the ways how to optimize its properties.*

Keywords: Charge Pump, Voltage Gain, Efficiency, NVM Test Modes.

1. Introduction

Test modes and methods are discussed e.g. in [1], above all we can give an example of Sector/Block/Mass modes, parallel programming, redundancy and reference matrix and internal nodes analysis.

Beside the necessary digital and control hardware (such as decoders, matrix drivers, etc.), there is also a need of powerful and efficient high-voltage generator.

The HV generator has to meet several criteria for the purpose of NVM measurement and test: adjustable output voltage possibly (to serve for Sector/Block/Mass Write or Erase modes), selectable current output drive capability, controlled slope of HV rise.

From design scope, efficiency plays main role. Charge Pump efficiency is reduced by many phenomena. Relatively strong effect has threshold voltage of used transistors or diodes. This paper is concentrated on optimizing of properties of proposed variant Charge Pump, as well.

Dickson Charge Pump (DCP)
Well known Charge Pump architecture is Dickson Charge Pump (DCP) [2]. Equations for description and design of DCP are summarized in [3]. The output voltage depends on input voltage, number of stages and voltage gain of one stage.

Optimal value of voltage gain is equal to amplitude of clocks. But the stray capacitance of nodes reduces the voltage gain. Main effect on resulted value of output voltage has usually threshold voltage of used transistors. Especially for supply voltage lower than 1 V the threshold voltage limits implementation of Dickson Charge Pump. So sub-volt applications use another architectures of Charge Pumps [4], [5].

Generally used principle for threshold effect suppression is a change of connection of transfer transistor from diode mode to switcher mode [6]. So voltage drop between two nodes does not equal to the threshold voltage but is equal to the saturation voltage of channel. Cross-coupled Charge Pump is well known architecture that uses this principle. Another variant is proposed and optimized.

Proposed variant of Charge Pump

Proposed variant of Charge Pump uses 2-phase clocks. One cell (stage) as a basic building block of this Charge Pump is shown on Fig. 1. The cell consists of two inverter totems (M_1, M_2 and M_3, M_4), bias transistor (M_5) and transfer capacitor (C_T).

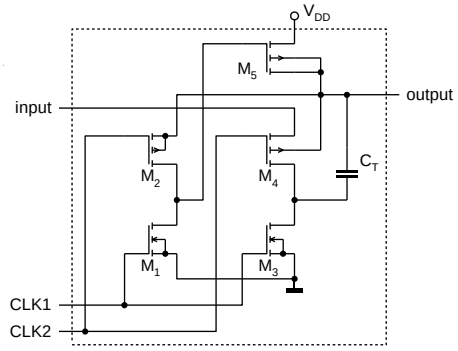

Fig. 1. One cell (stage) of proposed Charge Pump.

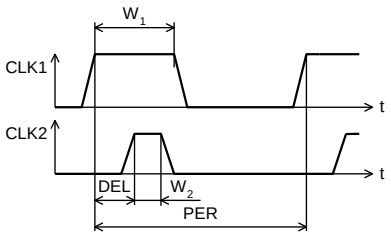

Fig. 2. Waveforms of 2-phase clocks.

The first inverter M_1, M_2 is driven by signal CLK2. This inverter controls gate voltage for bias transistor M_5. The second inverter M_3, M_4 is driven by signal CLK1. This inverter connects transfer capacitor C_T to ground or cell input. So transfer capacitor is pre-charged to V_{DD} in first clock phase and then transfer capacitor is connected between input and output nodes in second clock phase. Thus internode voltage (so called voltage gain) ideally equals to V_{DD}.

The clocks signals which are used for driving of both inverters have overlapped character as is drawn on Fig. 2. Symbols W_1 and W_2 mark widths of pulses of both clock signals. DEL marks the delay between rising edges of the CLK1 and CLK2 signals. PER is the period of both clock signals.

Setting of W_1, W_2 and DEL parameters is crucial for the best ratio between values of output voltage and resulting efficiency.

2. Simulations

6-stage Charge Pump according to Fig. 3 was used to simulate. Clocking signal is buffered by strong buffers (invertors). The last stage is connected to the detector based on transistor M_D. Resistor R_L a capacitor C_L model output load. Symbol I_S marks the consumed current. Output voltage at load is marked V_{OUT}.

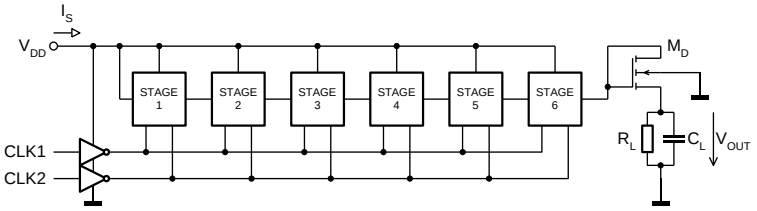

Fig. 3. Simplified schematic diagram of simulated Charge Pump.

Firstly, the optimal value of DEL value was found. CLK1 pulse width $W_1 = 24$ ns was selected as starting value according to the period of the clock signals.

Consequently DEL value was swept for various values of CLK2 pulse width W_2. See Fig. 4. The best value of efficiency $\eta = 12.2$ % was located for case DEL = 0, $W_2 = 10$ ns with output

voltage V_{OUT} = 4.036 V. But the maximal value of output voltage V_{OUT} = 4.107 V with efficiency η = 10.0 % was located for case DEL = 0, W_2 = 24 ns.

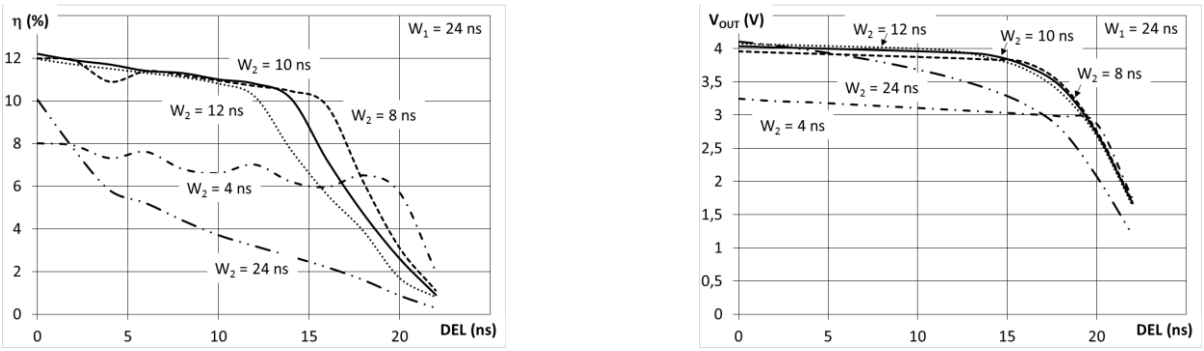

Fig. 4. a) Graph of efficiency, b) Graph of output voltage as functions of W_2 and DEL.

One important result was implied from the first simulation batch. Maximal value of efficiency was in case then DEL = 0 ns. So edges of both clocks must have started simultaneously.

Table 1. Parameters used for simulations (6-stage Charge Pump).

Parameter	Value
Clock frequency and temperature	f = 20 MHz (period PER = 50 ns), t = 27 °C.
Supply voltage, amplitude of clocks	V_{DD} = 0.7 V, V_{CLK} = 0.7 V.
Capacitance of transfer capacitors	C_T = 5 pF.
Load	C_L = 300 pF, R_L = 2.8 MΩ.
Buffers transistors (L = 0.1 μm)	NMOS_HVT: W = 5 μm, PMOS_HVT: W = 12.5 μm.
Cell transistors (L = 0.1 μm)	NMOS_HVT: W = 0.5 μm, PMOS_HVT: W = 1.25 μm.
Detector transistor	Native NMOS_NA18 (L = 0.8 μm, W = 20 μm).

Secondly, the simulations with variable W_1 (width of CLK1 pulse) were performed as is shown in Fig. 5. The best value of efficiency η = 13.3 % was for case W_1 = 36 ns, DEL = 0, and W_2 = 10 ns, but the output voltage had value V_{OUT} = 3.907 V only.

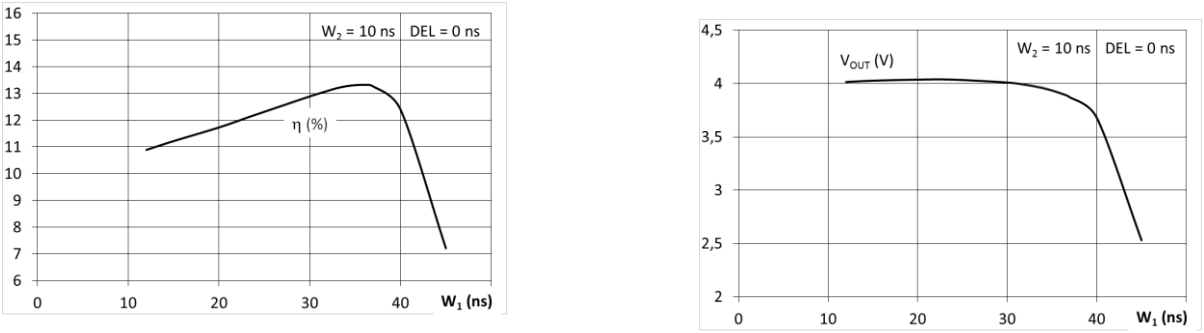

Fig. 5. a) Graph of efficiency b) Graph of efficiency and output voltage as functions of W_1.

The case W_1 = 24 ns, DEL = 0, W_2 = 10 ns was selected as a compromise between optimal values of the output voltage and efficiency. The ramp of the output voltage for this case is documented on Fig. 6. Rise time had value t_R = 74.3 μs.

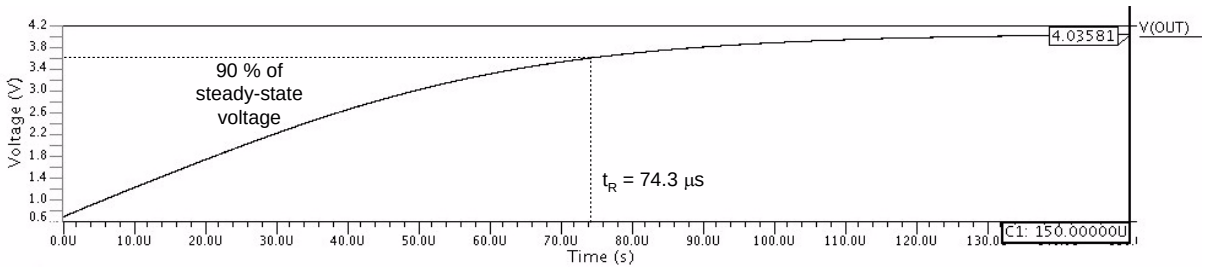

Fig. 6. Ramp of output voltage (W_1 = 24 ns, W_2 = 10 ns, DEL = 0).

3. Results

Maximal value of the output voltage V_{OUT} = 4.036 V with efficiency η = 12.2 % has been achieved. These results were obtained for CLK1 pulse width W_1 = 24 ns when CLK2 pulse width was W_2 = 10 ns and delay had value DEL = 0 ns. W_2 value may vary from 8 to 12 ns but value of efficiency varies very small.

4. Discussion

Optimizing of proposed Charge Pump was performed based on previously documented simulations.

Although maximal values of output voltage and efficiency are obtained for different values of timing parameters, these maxima are relatively close.

The important advantage of proposed variant of Charge Pump is in fact, that both clock signals are derived from same base clock. Both clock signals have simultaneous rising edges. The width of each clock signal may be simply tuned by a delay network.

Future work will be focused to the more complex circuit including clock generator to optimise. So we will find global efficiency of proposed Charge Pump.

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