Fast Demodulator for Asynchronous Sigma-Delta Modulator Signals

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Abstract. *Asynchronous sigma-delta modulator (ASDM) is closed-loop nonlinear system that transform the information in the amplitude of a bounded input signal into time information in the output signal, without suffering from quantization noise such as in synchronous sigma-delta modulators. This is an important advantage with many interesting applications. This paper investigates the commonly used asynchronous sigma–delta modulator, which consists of a Schmitt trigger and a continuous-time loop filter. Analysis is presented to accurately describe the properties of such modulator. The new circuit for fast demodulation of modulated signal is also described. The theoretical derivations were compared with simulation and measuring results. The presented circuits were analyzed, simulated, constructed and measured.*

Keywords: Asynchronous sigma-delta modulator, Pulse-width modulator, Demodulator, Digital-analog converter, Signal transmission

1. Introduction

Power requirement and dissipation due to analog to digital conversion as well as to wireless transmission are major limitations in the implementation of e.g. human implants or wireless EEG (Electro Encephalographic) signal measuring. Uniform sampling in the analog to digital converters (ADCs) requires synchronous implementation with a common clock shared with the digital signal processor. The need for a clock is a source of power consumption. In contrast, asynchronous circuits are not governed by a clock and consume low power. The elimination of clocks in these circuits also reduces device sizes and cuts electromagnetic interference (EMI) significantly. Due to these desirable properties, ASDMs have been proposed for data acquisition in bio-monitoring systems [1, 2]. An ASDM block diagram (Fig. 1) includes several functional blocks: an summation block, integrator, hysteretic comparator and a switch. The integrator output and switch output are shown in Fig. 2. It is a pulse width modulated (PWM) square wave of period T with a pulse-width t_1. The duty cycle *Duty* is proportional to the value of the input signal. Moreover, also the period T of the asynchronous modulator output depends on the input voltage.

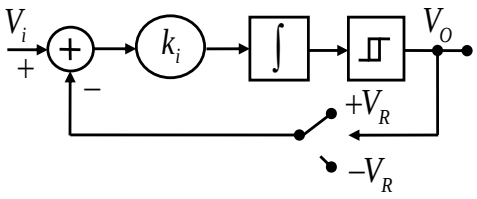

Fig. 1. The block diagram of the first order asynchronous sigma-delta modulator

Assume the band limited input voltage V_i ($|V_i|<V_R$). The output of the integrator V_{int} is (slope S_1, start from t_k to t_{k+1})

$$V_{int}(t_{k+1}) = k_i \int_{t_k}^{t_{k+1}} (V_i(t) + V_R)dt + V_{int}(t_k) \tag{1}$$

for $V_i(t)=V_i$ (constant input voltage) the time t_1 for $V_{int}(t_k)=-h$ and $V_{int}(t_{k+1})=h$ and time t_2 is

$$t_1 = t_{k+1} - t_k = \frac{Hys}{k_i\left(V_i + V_R\right)}; \quad t_2 = t_{k+2} - t_{k+1} = \frac{Hys}{k_i\left(V_R - V_i\right)} \tag{2}$$

and combining (2) and (3) output period T, frequency f and duty cycle D is

$$T = t_1 + t_2 = \frac{Hys}{k_i}\left(\frac{2V_R}{V_R^2 - V_i^2}\right); \quad f = \frac{1}{T} = \frac{k_i}{Hys}\left(\frac{V_R^2 - V_i^2}{2V_R}\right); \quad D = 100\frac{t_1}{t_1 + t_2} = 100\frac{t_1}{T} = 100\frac{V_R - V_i}{2V_R} \tag{3}$$

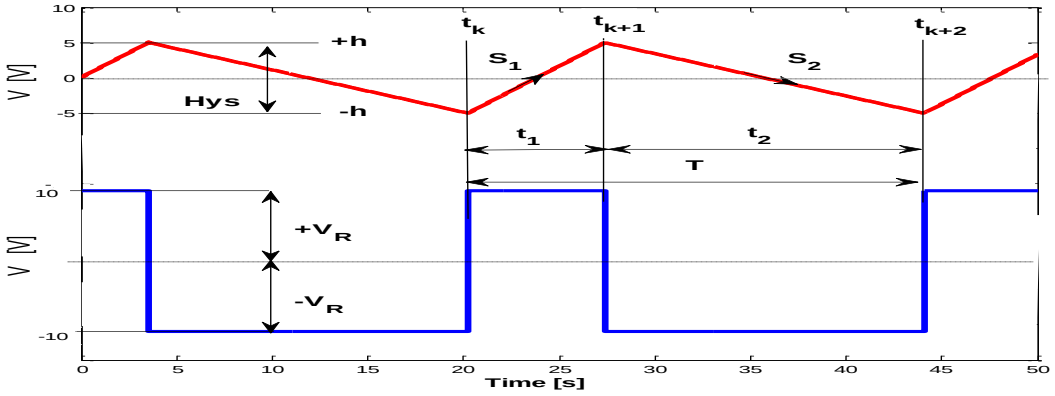

Fig. 2. The signals of the ASDM for V_i = 4 V, V_R = ±10 V, h = 5 V, Hys =10 V and k_i = 0.1. Integrator output $y(t)$ (top), switch output (bottom) versus time. S_1 and S_2 slopes on the integrator output signal

2. Modulator

The circuit diagram of the simple, first order ASDM (based on operational amplifiers) and demodulator with voltage output is shown in Fig. 3.

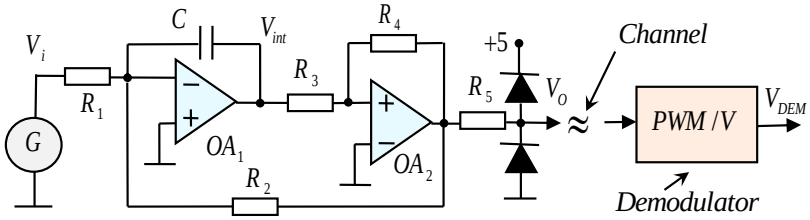

Fig. 3. The circuit diagram of the simple, first order ASDM (R1=R2=R3=R5=10 kΩ, R4=100 kΩ, C=100 nF, VR= 10.5 V, Hys=2.3 V, OA=TL072) signal transmission by different type of channel and demodulation by PWM/V block. V_i analog input voltage (from generator), V_{int} integrator output, V_0 output of modulator and V_{DEM} demodulated output voltage.

Instead k_i in eq. (1)-(4), for ASDM with operational amplifiers, k_i is substituted by $1/RC$, therefore

$$t_1 = RC\frac{Hys}{V_i + V_R}; \quad t_2 = RC\frac{Hys}{V_R - V_i}; \quad f = \frac{1}{t_1 + t_2} = \frac{1}{T} = \frac{V_R^2 - V_i^2}{2 \cdot RC \cdot Hys \cdot V_R} \quad [\text{s, Ω, F, V}] \tag{4}$$

The calculated and measured results of ADSM for R_1=R_2=R_3=R_5=10 kΩ, R_4=100 kΩ, C=100 nF, V_R= 10.5 V, Hys = 2.3 V are shown in Fig. 4. From this figure can be seen almost the same calculated (dash lines) and measured (solid lines) duty and frequency dependencies versus input voltage. The measured (and calculated) duty cycle D_{CALC} versus V_i (for $V_i \in \langle -9 \div 9 \rangle$ [V]) can be approximated as

$$D_{CALC} = 50 - 4.83 \cdot V_i \quad [\%, \text{V}] \tag{5}$$

and measured (and calculated) output frequency f_{CALC} versus V_i are

$$f_{CALC} = 2.4 - 0.0216 \cdot V_i^2 \qquad \text{[kHz, V]} \qquad (6)$$

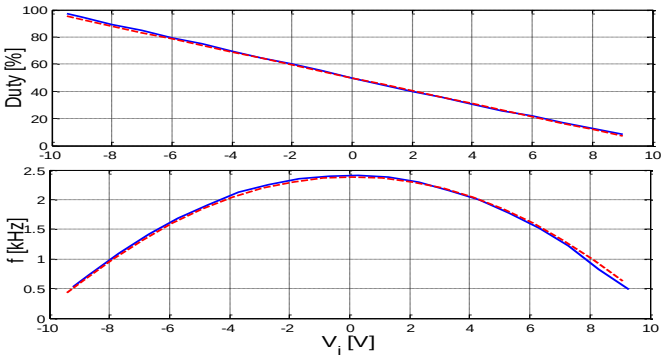

Fig. 4. The calculated (dash line) and measured (solid line) duty (top) and frequency (bottom) versus V_i for simple ASDM according Fig. 3, (for $V_i \in \langle -9 \div 9 \rangle$ [V])

3. Fast Demodulator

Signals with pulse-width modulation (or ASDM signals) are very easy to demodulate by lowpass filter but with slow response. This approach can be modified by using counters and digital-analog (D/A) converter. This principle of the PWM demodulation is used for fast demodulation of ASDM signal. It is important to note that PWM signal generated by ASDM change booth – pulse width and also frequency. Output of the fast demodulator is updated every rising edge of input signal. The LTC2644 IC's (PWM/V converter, see Fig. 5) is used for fast demodulation [3, 4]. This IC's is not sensitive for frequency changing. After each rising edge of input signal, the IC's calculates the duty cycle based upon the pulse width and period and updates D/A output (within 8 μs for 12-bit). The demodulated output voltage V_{DEM} can be calculated by the following equation

$$V_{DEM} = V_{REF} \cdot t_1 / T \qquad \text{[V, s]} \qquad (7)$$

where V_{REF} is 2.5 V internal reference voltage (or external reference voltage) and t_1 is width of PWM signal and T is period of PWM signal.

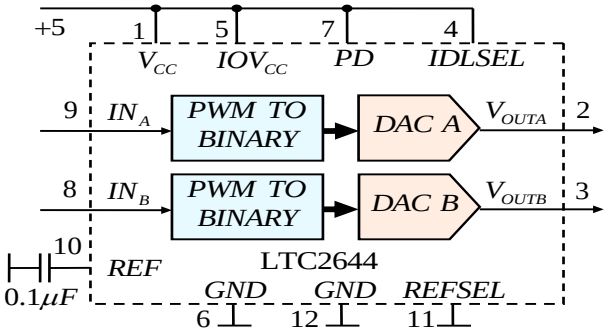

Fig. 5. The circuit diagram of 2 channel fast PWM/V demodulator - LTC2644. PWM input pins 8 and 9 are inputs, pins 2 and 3 are voltage outputs.

4. Measuring Results

The fast demodulator for ASDM signal was tested for analog signal transmission and demodulation. The time evolutions of the signals are shown in Fig. 6. In this figure are shown signals on input, integrator output, ASDM output and demodulated output. The frequency of

input signal: 200 Hz. The maximal frequency of the ASDM: approx. 2.5 kHz (for $V_i = 0$) and minimal approx. 1.7 kHz (for $V_i \approx \pm 5$ V).

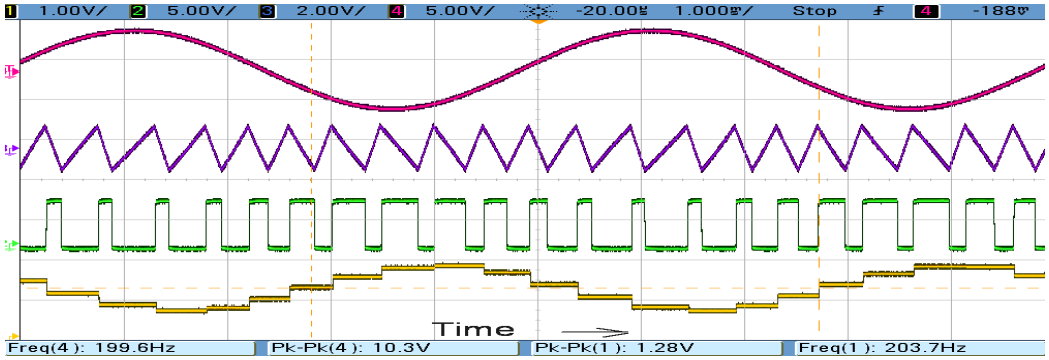

Fig. 6. The example of analog signal transmission by means of ASDM. From top to bottom (time signals): Input signal V_i from generator; output of the integrator V_{int}; output of the modulator V_0; demodulator output V_{DEM}

5. Conclusion

In this paper the fast demodulator for ASDM was described. This circuit can be used in different applications e.g. in biomedical engineering, optically coupled systems, sensors and other industry applications. Very important is fast demodulation of ASDM (demodulation in one period of ASDM signal) without using low-pass filter. The presented systems were described, simulated, constructed and measured. The paper illustrates a good match between theory and measuring results.

Acknowledgements

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