Integral Nonlinearity Correction of Multi-Range ADC by Iterative Applying of Multi-Resistors Divider

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Abstract. *The method of testing points generation for identification and correction of integral nonlinearity of high performance ADC is developed. The proposed method is based on averaging all voltages of multi-resistors voltage divider. The main idea of proposed method is in comparison results of analog to digital conversion obtained on different ranges of tested ADC for the same input signals. It is investigated influence of resistors' error and random error of ADC on residual error of integral nonlinearity correction for proposed method.*

Keywords: Integral nonlinearity, Multi-resistor voltage divider, Residual error

1. Introduction

Implementation of digital signal processing algorithms and computer systems in all fields of our life results in implementation of analogue-to-digital converters (ADC) as necessary a component of modern measurement systems. In some cases the ADC's metrology parameters determine the characteristics of whole measurement system. Particularly, this point is actual for measurement systems of electrical quantities. Therefore improving the ADC is actual task for accuracy increasing.

The market of DC precision ADC is covered by converters based on sigma-delta modulators SDM [1, 2]. High accuracy of these components is provided by implementation of null setting and calibration methods. These methods provide decreasing of additive and multiplicative components of conversion error. Therefore, the error of conversion results in determination of the following errors: calibration signal source, multiplexer and residual ADC's error. The main significant component of this residual ADC's error is their integral nonlinearity. For example, the maximum allowable integral nonlinearity of 24-bit ADC AD7714 [3] is 15 ppm. This nonlinearity corresponds to 16-th bit, therefore approximately 8 least significant bits (LSB) are priory inaccurate and excessive. Therefore, for this ADC integral nonlinearity should be corrected when we need accurate result than 15 ppm. In the same case, the noise level of this ADC does not exceed of 2,5 LSB. Therefore, we have approximately 5,5 stable bits, which cannot to be used because their inaccuracy. Also there is such precise measurement method as substitution measurement method [4]. The accuracy of measurement results for this method implemented on ADC is defined by ADC's integral nonlinearity [5]. So correction of ADC's integral nonlinearity brings accuracy improvement of measurement results.

In [6] the method of ADC's integral nonlinearity identification in the set of testing points conventionally called as basic method was proposed. This method provides generation the set of testing points, which corresponds to the number sequence $\frac{1}{N}U_R$ (U_R – range of connected ADC) with integer N. This implies that all generated testing points are grouped in the lower

half of the ADC's range. Investigation of nonlinearity correction methods show that residual error is proportional to the density of testing points [7, 8]. It brings inefficiency of this method for signals, which corresponds to the top half of the ADC's range. Finally, basic method implementation for ADC's nonlinearity correction brinks that residual error for signals from top half of the ADC's range is more than 10 times greater than this error for signals from lower half of the range [6].

Proposed in [9, 10] method of testing points generation by direct measurement of the voltages on serially connected resistors of multi-resistors divider. This method implements basic method for nonlinearity of lower half of the ADC's range. Than it is measured voltages on serially connected resistors: R_1; R_1 and R_2; … $R_1 ... R_{N/2}$ (totally $N/2$ voltages, where N - total number of resistors in multi-resistors divider). The error of measurement results of all these voltages is small because they are in lower half of the ADC's range, where basic method is effective. Mainly error of these voltages is defined by ADC's random error. Measured voltages are used as testing points for all lower ranges of ADC. This method provides approximately uniform distribution of testing points for all lower ranges of ADC but its accuracy is significantly lower in comparison with basic method because of error accumulation.

The main goal of this work is development and investigation of method of ADC's integral nonlinearity identification and correction for multi range ADC which provides iterative implementation multi-resistors divider on different ranges of tested ADC.

2. Approach of Testing Points Generation

The basic of proposed method of testing points generation is based on analog to digital conversion of output signals of voltage divider consisting of N serially combined resistors $R_1, R_2, ..., R_N$, connected to reference power source U_{REF}. The measurement circuit is shown in Fig. 1. According to Kirchhoff voltage law, we have the following equation

$$U_{REF} = \sum_{i=1}^{N} U_{R\,i} \ , \tag{1}$$

where $U_{R\,i}$, $i = \overline{1, N}$ is voltage of appropriate resistors of the divider.

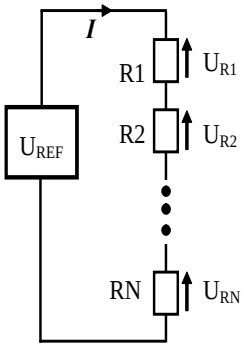

Fig. 1. Circuit of N -resistors voltage divider.

The average voltage of all resistors of the divider $\overline{U}$ could be computed as:

$$\overline{U} = \frac{1}{N} \sum_{i=1}^{N} U_{R\,i} \ . \tag{2}$$

Taking into account eq. (1), the eq. (2) can be presented as

$$\overline{U} = \frac{U_{REF}}{N} \ . \tag{3}$$

It means that average voltage of all resistors of the divider $\overline{U}$ does not depends of voltages of separate resistors. In addition, according to Ohm's law, the resistances of these resistors does not influence on average voltage.

Equivalently, we have indirect measurement describing by function $y = h(x)$, where $y \equiv \overline{U},\ x \equiv U_{REF}\ \ h(x) \equiv \frac{x}{N}$. Therefore, absolute error of measurement result is Δy [11]:

$$\Delta y = h'(x) \cdot \Delta x \ , \tag{4}$$

where $h'(x)$ – derivative of function $h(x)$; Δx – absolute error of argument.

Taking into account, that N is natural number, the eq. (4) could be convert to

$$\Delta_{\overline{U}} = \frac{\Delta_{U_{REF}}}{N} \ , \tag{5}$$

where $\Delta_{\overline{U}}$ - absolute error of average voltage $\overline{U}$; $\Delta_{U_{REF}}$ - absolute error of power source U_{REF}.

The relative error of average voltage $\overline{U}$ – $\delta_{\overline{U}}$ is

$$\delta_{\overline{U}} = \frac{\Delta_{\overline{U}}}{\overline{U}} 100\% = \frac{\frac{\Delta_{U_{REF}}}{N}}{\frac{U_{REF}}{N}} 100\% = \frac{\Delta_{U_{REF}}}{U_{REF}} 100\% = \delta_{U_{REF}} \ , \tag{6}$$

where $\delta_{U_{REF}}$ - relative error of power source U_{REF}.

Taking into account (6), the next intermediate conclusion should be made: the error caused by measurement converter based on multi-resistors voltage divider with averaging voltages of all resistors is trend to zero. It is provide the opportunity of generation the set of testing signals for ADC with exactly predefined ratio.

In the case of ADC calibration by power source of the divider U_{REF}., the average voltage $\overline{U}$ as testing point for identification ADC's integral nonlinearity can be used.

So, as it is shown, that the multi-resistors voltage divider provides precision identification of ADC's integral nonlinearity in one testing point without using of precision components. Proposed method is called as basic method [6] and they provides increasing of number of generated testing points by choosing N. Since N has the set of natural divisors $\{m_1,\ldots,m_t\}$, it is the set of natural numbers $\{k_1,\ldots,k_t\}$, which satisfy of a claim $N = m_i \times k_i;\ i = \overline{1,t}$. It is allowed to conversion of voltages on the cascades of serially connected resistors $k_i,\ i = \overline{1,t}$ corresponding to eq. (1). Therefore, the integral nonlinearity of ADC can be computed in accordance to the set of t voltages:

$$\overline{U}_i = \frac{U_{REF}}{N} k_i = \frac{U_{REF}}{m_i}; \quad i = \overline{1,t} \ . \tag{7}$$

The error of all these voltages is corresponded to eq. (6), and only one reference voltage source can be used.

3. Proposed Method of Generation Testing Points

According to the methodology, which was proposed in [6] it is proposed to generate testing points for nonlinearity identification of lower ranges of multi range ADC (in the simplest case for double range ADC) as average voltage for the same combinations of serially connected resistors, which implements basic method for highest range of ADC. It provides getting the set of testing points, which are proportional to calibration voltage of highest range of ADC with coefficient predefined as the deviation of integer numbers. In this case the relative error of all generated testing points is equal to relative error of reference voltage source. The calibration of all lower ranges is held by the voltage of serially connected resistors directly measured on the highest range. Taking into consideration that lover ranges are at least two times less than highest range the distribution of generated testing points for lover ranges will be evenly then it is provided by basic method for higher range. Besides the most generated testing points (besides calibration points) are more accurate than testing points generated by direct measurement the voltages on serially connected resistors of multi-resistors divider [9, 10]. So this method provides generation the same set of testing points as it is generated by basic method [6] but these points are situated higher in the range than it is for basic method. The total number of generated testing points is defined by the number of integer dividers of N. For example if $N=12$ then this method provides generation five testing points using single channel DC voltage source and error of resistors should not influence on these points.

4. Investigation of the Residual Error

Investigation of the residual nonlinear error by experimental way demands extremely precision equipment with error of 3…5 times less then expected residual nonlinearity and it corresponds to 0,5 ppm. Besides, it is necessary to have the opportunity to set the level and view of ADC's nonlinearity with the same error level. So, it is proposed to make investigation of the proposed method by simulation and evaluate influence of resistors' error and ADC's noise on residual nonlinear error for different nonlinearity functions. Generally, the methodology of investigation results in emulation of integral nonlinearity by the set of curves and it's computing according the proposed method. The difference between emulated and computed curves is the error for analysis. Generally the algorithm of investigation is similar to the same in [6, …, 10]. Its implementation for the set of different curves, which describes nonlinearity of ADC, shows that maximal residual error of nonlinearity correction is on the largest segment between generated testing points. The value of this maximal residual error is proportional to noise level of tested ADC.

5. Conclusions

Investigation of the proposed method of integral nonlinearity identification and correction for lower range of ADC gives us the following conclusions:

- influence of resistors' error of the voltage divider on residual error is commensurable with ADC's resolution and it is neglecting small in comparison with other errors;
- the influence of ADC's random error on residual error is dominating and proportional to its noise level with proportionality factor three for 12-resistors voltage divider;
- it is rational to provide even distribution of testing points via the range of tested ADC for residual error minimization.

The weak sensitivity of proposed method to resistors' error and ADC's noise provides the

opportunity of its implementation for metrology verification subsystem [12] of ADC using single channel reference voltage source. The error of such metrology verification is mainly defined by error of implemented reference voltage source, therefore, metrology support of such metrology verification subsystem is reduces to metrology verification of reference voltage source. It provides the opportunity to embed this metrology verification subsystem with reference voltage source into ADC.

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