MEASUREMENT SCIENCE REVIEW, **16**, (2016), No. 5, 260-265

ISSN 1335-8871

MEASUREMENT SCIENCE REVIEW

Journal homepage: http://www.degruyter.com/view/j/msr

Efficiency of Innovative Charge Pump versus Clock Frequency and MOSFETs Sizes

David Matoušek[1], Jiří Hospodka[1], Ondřej Šubrt[2, 1]

[1]*Department of Circuit Theory, FEE CTU in Prague, Technicka 2, 16627, Prague, Czech Republic, matoudav@fel.cvut.cz*
[2]*ASICentrum, a company of the Swatch Group, Novodvorska 994, 14221, Prague, Czech Republic*

Charge pumps are circuits that produce the voltage higher than supply voltage or negative voltage. Today, charge pumps became an integral part of the electronic equipment. The integration of charge pumps directly into the system allows manufacturers to feed a complex system with many specific power requirements from a single source. However, charge pump efficiency is reduced by many phenomena. This paper is focused on the question of efficiency of proposed variant of the charge pump. In this article, the efficiency dependence on a number of stages, output current, clock frequency and MOSFETs sizes was simulated by Eldo. The aim of this study is to determine the MOSFETs sizes and theirs influence to efficiency and the output voltage. Complex optimization of the charge pump circuit will follow in further text.

Keywords: 2-phase Charge Pump, non-volatile memory, efficiency, switch size determination.

1. INTRODUCTION

The Dickson Charge Pump (DCP) [1] belongs to well-known charge pump architectures. The design equations for this DCP are summarized in [2]. The differential voltage ΔV between nodes n and $n+1$ is

$$\Delta V = V_{n+1} - V_n = V_S - V_T \,, \tag{1}$$

where V_S is the voltage swing at each node due to capacitive coupling from the clock [2], V_T is the threshold voltage of the diode-connected transfer transistors.

The optimal value of the voltage swing equals to the amplitude of clocks. But the stray capacitance of node reduces voltage [2] swing as follows

$$V_S = \left(\frac{C_T}{C_T + C_S}\right) \cdot V_{CLK} \,, \tag{2}$$

where V_S is the voltage swing, C_T is the transfer capacitance, C_S is the stray capacitance, V_{CLK} is the amplitude of clocks.

Since the no-load output voltage applies according to [2]

$$V_O = V_{IN} + N \cdot (V_S - V_T) - V_T \,, \tag{3}$$

where V_O is the no-load output voltage, V_{IN} is the input voltage, N is the number of stages, V_S is the voltage swing, V_T is the threshold voltage.

The equation (3) shows the output voltage in an ideal situation when the pump is not delivering any output load current. The effect of the load current is described by [2]

$$V_{OUT} = V_O - I_{OUT} \cdot R_S \,, \tag{4}$$

where V_{OUT} is output voltage at load, V_O is the no-load output voltage, I_{OUT} is the load current ($I_{OUT} \geq 0$), R_S is the internal resistance of the charge pump.

The internal resistance of the charge pump depends on the number of stages N, transfer capacitance C_T, stray capacitance C_S and clock frequency f [2]

$$R_S = \frac{N}{(C_T + C_S) \cdot f} \,, \tag{5}$$

The threshold voltage of used transistors has usually the main effect to resulted value of the output voltage. It limits the DCP implementation, especially for supply voltage lower than $1\,V$. Therefore, sub-volt applications use other architectures of charge pumps [3], [4].

A change of connection of transfer transistor from diode mode to switching mode [5], [6], [7] is generally used principle for threshold effect suppression. Thus the voltage drop between two nodes is not a threshold gate-source voltage but the saturation voltage of channel only.

DOI: 10.1515/msr-2016-0032

2. SUBJECT & METHODS

Proposed variant of the charge pump [8] uses the 2-phase clock. One cell as the basic building block of this charge pump is shown in Fig.1. The cell contains five transistors (M_1 to M_5) and transferring capacitor (C_T).

This cell is driven by overlapped clock signals according to Fig.2. Falling edges both clock signals start simultaneously.

In the first phase ($CLK1 = V_{DD}$, $CLK2 = V_{DD}$), transistors M_1, M_3 and M_5 are ON. Thus transferring capacitor C_T is biased to supply voltage V_{DD}.

In the second phase ($CLK1 = GND$, $CLK2 = GND$), transistors M_2 and M_4 are ON. Thus transistor M_2 holds bias transistor M_5 in the disconnected state. Transistor M_4 connects the transferring capacitor C_T between input (output of the previous cell) and output, now. Therefore, the input voltage is increased by a voltage of transferring capacitor from the biased phase.

In the last phase ($CLK1 = GND$, $CLK2 = V_{DD}$), all transistors are OFF.

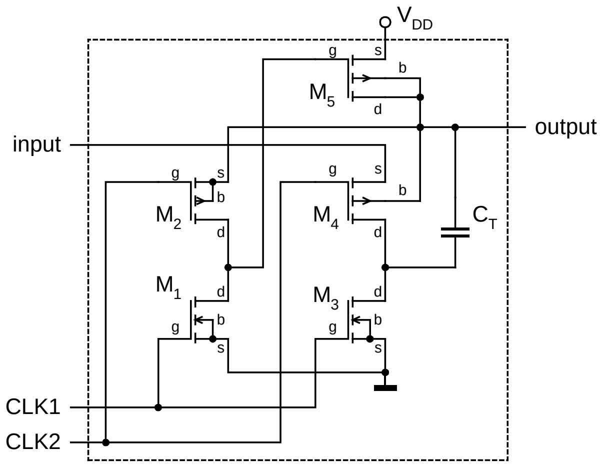

Fig.1. One cell of the proposed charge pump [8].

Used clock signals have overlapped character as is shown in Fig.2. Symbols W_1 and W_2 mark width of pulses both clock signals. *PER* is the period of both clock signals. The optimal W_1, W_2 values for the best ratio between the output voltage and resulted efficiency were estimated in the previous contribution [8] as $W_1 = 24$ *ns* and $W_2 = 10$ *ns* for *PER* = 50 *ns*.

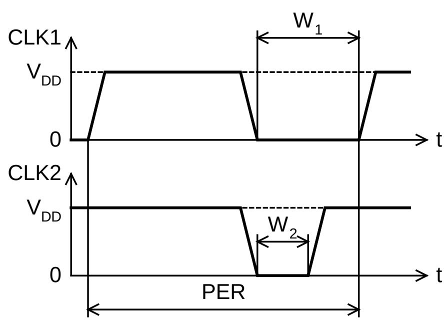

Fig.2. Waveforms of 2-phase clocks.

A. Proposed design algorithm

The design rules for initial basic parameters estimation of proposed charge pump may be summarized to undermentioned steps.

For illustration, we consider these charge pump specifications:

- power supply voltage $V_{DD} = 0.7$ V, minimal steady-state output voltage $V_{OUT} = 4$ V,
- output load capacitance $C_L = 300$ pF, output current $I_L = 4$ μA,
- maximal output voltage ramp-up time $t_r = 150$ μs.

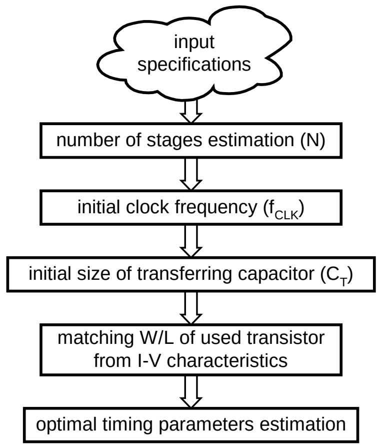

Fig.3. Design-flow diagram.

The number of stages: Initial estimation of number of stages N is calculated as ratio of the output voltage V_{OUT} and the voltage gain of one stage V_E (ideally, this gain has the same value as supply voltage):

$$N = \frac{V_{OUT}}{V_E} = \frac{4}{0.7} \approx 6 \tag{6}$$

The initial clock frequency f_{CLK}: Initial clock frequency was assumed as $f_{CLK} = 20$ *MHz*.

The initial size of transferring capacitor C_T: Value of transfer capacitance C_T may be calculated from known load capacitance C_L, number of stages N, ramp-up time t_r and clock frequency f_{CLK} [2]:

$$C_T = C_L \frac{N}{t_r \cdot f_{CLK}} = 300 \cdot 10^{-12} \frac{6}{150 \cdot 10^{-6} \cdot 20 \cdot 10^{6}} = 0.6\,\text{pF} \tag{7}$$

The W/L of used transistors: The MOSFETs M_3 to M_5 and M_D used for transfer charge should have conductance at least ten times higher than conductance matched to the output current [2], thus their initial size must be estimated from I-V characteristics [8]. The MOSFETs M_1 to M_2 may cause losses of charge, but these MOSFETs are used for driving transistor M_5 only. Therefore, these transistors may be relatively narrow [8].

Parameters of used transistors are summarized in Table 1.

Transferring capacitor C_T is realized as transistor M_{CT}, its capacity was calculated by derivation of I-V characteristics. M_{BUFA} and M_{BUFB} are transistors from clock buffers. Models nmos_hvt and pmos_hvt correspond to "high voltage" transistors with a relatively high value of V_T. Model nmos_na18v corresponds to the native transistor for 1.8 V technology.

Table 1. Parameters of transistors.

Transistor	W (μm)	L (μm)	model
M_1	0.2	0.1	nmos_hvt
M_2	1	0.1	pmos_hvt
M_3	0.5	0.1	nmos_hvt
M_4	2.5	0.1	pmos_hvt
M_5	2.5	0.1	pmos_hvt
M_{CT}	30	10	nmos_hvt
M_D	20	0.8	nmos_na18v
M_{BUFA}	5	0.1	nmos_hvt
M_{BUFB}	12.5	0.1	pmos_hvt

The estimated area of the chip for the realization of proposed charge pump is listed in Table 2. where *N* is the number of stages, A_{STAGES} is the area for the realization of stages, A_{BUFDET} is the area for realization clock buffers and output detector, A_{TOTAL} is the area for realization proposed charge pump with required number of stages. The technological node corresponds to 100 nm.

Table 2. Estimated area for the realization of the charge pump.

N	A_{STAGES} (μm^2)	A_{BUFDET} (μm^2)	A_{TOTAL} (μm^2)
1	469	30	499
2	998	30	1028
3	1497	30	1527
4	1996	30	2026
5	2495	30	2525
6	2994	30	3024

Note, that area for realization clock buffers and output detector A_{BUFDET} has a constant value over a number of stages *N*. Namely, individual stages of the charge pump use common clock buffers.

The optimal timing parameters: The optimal timing parameters for clock frequency $f_{CLK} = 20\,MHz$ were estimated in previous contribution [8] as $W_1 = 24\,ns$ and $W_2 = 10\,ns$ for $PER = 50\,ns$. For other values of frequency, the timing parameters must be proportionally changed according to Table 3.

Table 3. Timing parameters for various value of clock frequency.

f_{CLK} (MHz)	PER (ns)	W_1 (ns)	W_2 (ns)
10	100	48	20
13.3	75	36	15
20	50	24	10
27	37	17.8	7.4
40	25	12	5

B. Study of clock frequency influence to efficiency and output voltage

The aim of this part of simulations is to determine the influence of clock frequency to efficiency primarily and output voltage secondarily.

Schematic diagram of simulated circuit is shown in Fig.4. This instance is 6-stage charge pump (N=6). A number of stages (i.e. cells) are changed for other instances only. Clock signals are buffered by strong buffers (inverters). Diode detector based on transistor M_D is connected to the last stage. Resistor R_L and capacitor C_L model resistive and capacitive parts of output load. Proposed charge pump was powered from $V_{DD} = 0.7\,V$ and both clock signals had amplitude $0.7\,V$, too. Symbol I_S marks consumed current. The output voltage at the load is marked V_{OUT}.

A number of stages N were varied from 1 to 6, clock frequency was set to values 10, 13.3, 20, 27, 40 MHz. Complex analyse for a number of stages varied from 1 to 6 was performed. But in this text, the results for variant N = 6 was chosen. Symbol I_L marks resistive part of output current.

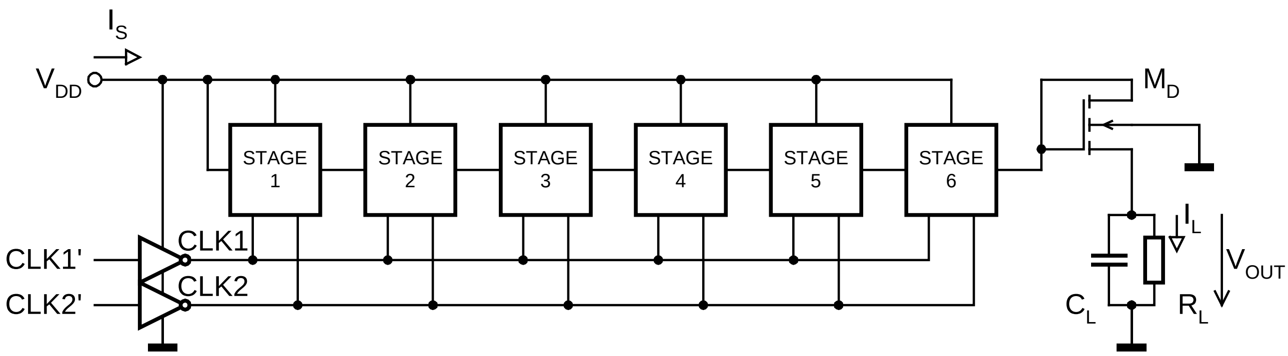

Fig.4. Simplified schematic diagram of the simulated charge pump for N=6.

Fig.5. shows that efficiency increases with increasing value of load current and decreasing value of clock frequency. Increasing the clock frequency leads to increasing power consumption, thus efficiency decreases with increasing clock frequency. While the power consumption for given clock frequency is relatively near a constant value and does not vary with output current. Therefore, efficiency increases with increasing load current.

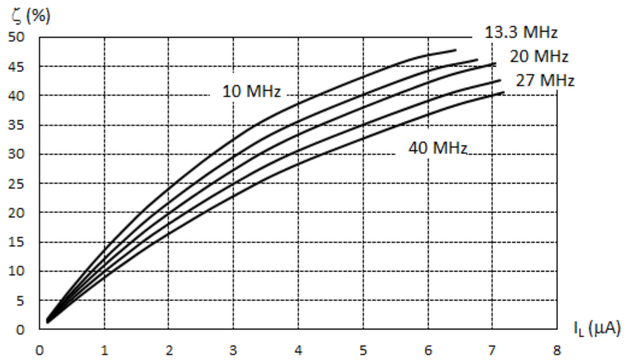

Fig.5. Efficiency as a function of I_L for N=6.

Fig.6. shows the output voltage variation with resistive part of output current I_L and clock frequency. Increasing the clock frequency will increase the amount of charge transferred over a given time interval, thus output voltage has a higher value. The presence of a fixed capacitive load leads to increasing no-load output voltage with increasing clock frequency.

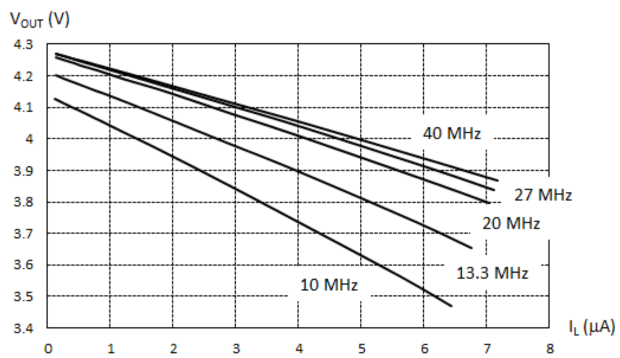

Fig.6. Output voltage as a function of I_L for N=6.

Total efficiency was calculated as ratio of the output power P_{OUT} in steady-state (8) and the total consummated power from power supply P_{IN} (9) according to (10)

$$P_{OUT} = V_{OUT} \cdot I_{OUT} = \frac{V_{OUT}^2}{R_L}, \tag{8}$$

$$P_{IN} = V_{DD} \cdot I_S, \tag{9}$$

$$\zeta = \frac{P_{IN}}{P_{OUT}} \cdot 100\,\% = \frac{V_{OUT}^2}{V_{DD} \cdot I_S \cdot R_L} \cdot 100\,\%, \tag{10}$$

where V_{OUT} is the output voltage in steady-state, V_{DD} is the power voltage, I_S is the average value of current consumed from power supply including a current of clock buffers, R_L is the output load.

Efficiency is varied about 10 % (from 38.47 % at frequency 10 MHz to 28.64 % at frequency 40 MHz) for the nominal value of the output current $I_L = 4\ \mu A$. For the same conditions, the output voltage varies from 3.741 V to 4.051 V.

Simulation results are very similar for another number of stages of the charge pump. The situation is summarized in Table 4.

Table 4. Efficiency and output voltage for a various number of stages at output current 4 μA.

N	ζ(%)	V_{OUT} (V)
1	69.53 to 59.33	1.275 to 1.290
2	64.63 to 43.26	1.919 to 1.950
3	60.06 to 47.07	2.540 to 2.590
4	53.75 to 42.02	3.130 to 3.120
5	47.79 to 37.30	3.638 to 3.762
6	37.47 to 28.64	3.671 to 4.051

Values of efficiency are relatively low because proposed charge pump works at relatively low value of the power supply voltage (V_{DD} = 0.7 V).

C. MOSFET size influence to efficiency and output voltage

The aim of this part of simulations is to determine the influence of MOSFETs size to the efficiency and output voltage. Thus sizes of all transistors were swept in the second part of simulations. Only one parameter was changed, sizes of other transistors (according to Table 1.) were left unchanged. Output load was set to constant value R_L = 1 MΩ. These simulations were performed for 6-stage charge pump only at clock frequency 20 MHz.

Next, the seven options of simulations were performed to determine the influence of transistor dimensions.

Option 1: width of transistors M_4 and M_5 was swept from 0.5 μm to 50 μm. The size of these transistors has strong influence to both observed quantities (see Fig.7.) because these transistors have the main effect to transfer of charge in the first phase (biasing of C_T) and the second phase (transferring charge of C_T to output).

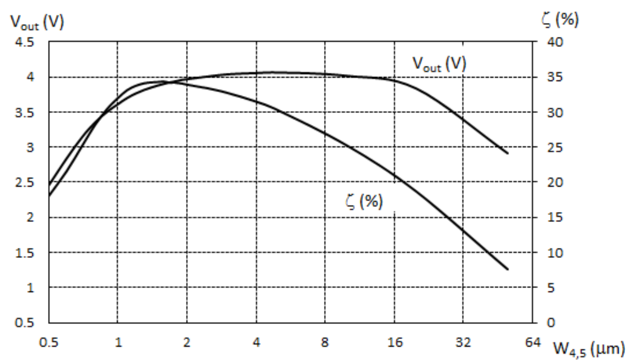

Fig.7. Option 1: Efficiency and output voltage as functions of $W_{4,5}$.

Option 2: width of detector M_D was swept from 0.5 μm to 50 μm. The size of the transistor M_D has the primarily influence to the efficiency (see Fig.8.) because this transistor determines the ratio of energy that is transmitted to load to the energy that is consumed from the power supply.

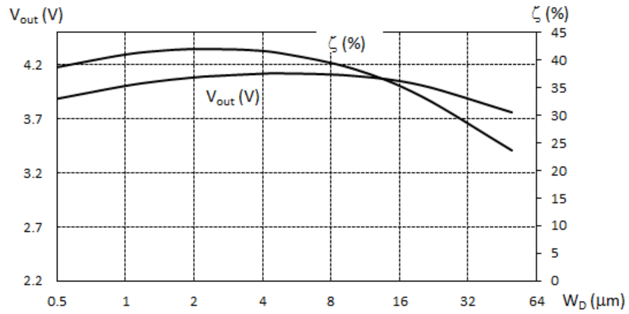

Fig.8. Option 2: Efficiency and output voltage as functions of W_D.

Option 3: width of transistor M_3 was swept from 0.2 μm to 10 μm. The size of the transistor M_3 has the primarily influence to the output voltage (see Fig.9.), because this transistor has significant effect to transfer of charge in the first phase (biasing of C_T).

Option 4, 5: widths of transistors M_1 and M_2 were swept from 0.2 μm to 10 μm or from 0.2 μm to 20 μm respectively. Increasing widths of these transistors lead to an increase of discharging process effect of the transfer capacitor C_T. Hence, transistors M_1 and M_2 must be narrowed, see Fig.10.

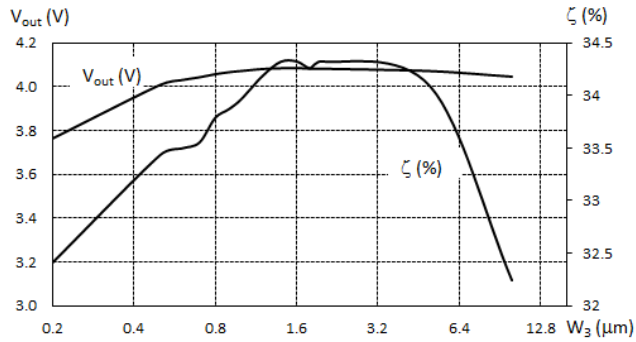

Fig.9. Option 3: Efficiency and output voltage as functions of W_3.

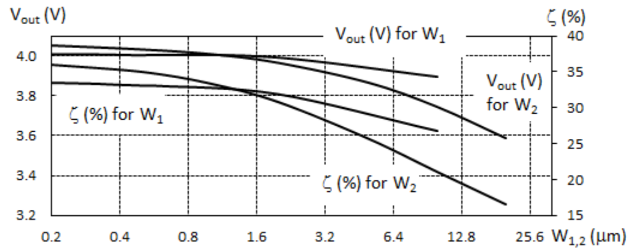

Fig.10. Option 4, 5: Efficiency and output voltage as functions of $W_{1,2}$.

Option 6: width of transistor M_{CT} was swept from 6 μm to 60 μm. The optimal size of the transistor M_{CT} is a compromise between efficiency and output voltage (see Fig.11.). Influence of variation in the capacity of transfer capacitor C_T has a strong effect on the internal resistance of the charge pump (thus this capacity has a strong effect on the output voltage). The optimal value of C_T capacity for maximizing efficiency is a more complex question. The main role plays value of C_S capacity for low values of C_T and increased power supply for high values of C_T.

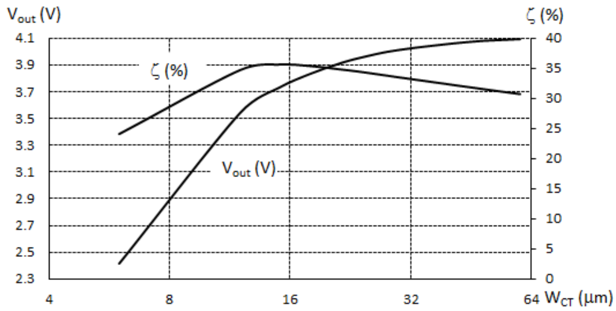

Fig.11. Option 6: Efficiency and output voltage as functions of W_{CT}.

Option 7: width of transistor M_{BUFA} was swept from 1 μm to 20 μm and simultaneously M_{BUFB} was swept from 5 μm to 100 μm. Maximal value of efficiency $\zeta = 33.67\ \%$ for $V_{OUT} = 4.006\ V$ occurs for $W_{BUFA} = 1\ \mu m$ and $W_{BUFB} = 5\ \mu m$. This variant isn't plotted because differences of values of efficiency and output voltage were relatively small. These transistors must be narrowed because increased conductance of wide transistor leads to increase switching current of these buffers.

3. RESULTS

Results from the simulations imply possibility for optimization efficiency of proposed charge pump. Values of efficiency and output voltage are $\zeta = 33.43\ \%$ and $V_{OUT} = 4.008\ V$ for original sizes of MOSFETs according to Table 1. and load R_L = 1 MΩ.

4. DISCUSSION

Study of efficiency and the output voltage versus clock frequency and MOSFETs sizing for proposed charge pump was performed. Parameters of MOSFETs and clock scheme were chosen according to a previous study [8]. Analyse was performed by Eldo simulator version 2010.2b. The Eldo is an SPICE-like simulator from Mentor Graphics Corporation.

The first part of simulations demonstrates that the efficiency increases with increasing load current and decreasing clock frequency. However, the dependency of the output voltage has opposite character, because the output voltage increases with decreasing load current and increasing clock frequency.

Results from the second part of simulations imply possibility for optimization efficiency of proposed charge pump. Effect of transistor sizing allows improving the efficiency about ten percent. Dimensions of transistors M_4, M_5, M_D and M_{CT} have the main effect on efficiency, M_3 has the important effect on the output voltage. Effect of other transistors has predictable character and we may neglect effect on the size of these transistors. Results from this study can be used for complex optimization study performed in the next period.

The validity of the presented results is limited to pre-layout simulations. Therefore, parasitic effects of higher orders (e.g. interlayer capacitance, metallic interconnection capacitance etc.) are neglected. These parasitic effects can have a significant influence on attainable results.

ACKNOWLEDGMENT

This work has been supported by the grant No. SGS14/191/OHK3/3T/13 of the CTU in Prague.

REFERENCES

[1] Dickson, J.F. (1976). On-Chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid-State Circuits*, 11 (3), 374-378.

[2] Pan, F., Samaddar, T. (2006). *Charge Pump Circuit Design*. McGraw-Hill Education.

[3] Palumbo, G., Pappalardo, D. (2010). Charge pump circuits: An overview on design strategies and topologies. *IEEE Circuits and Systems Magazine*, 10 (1), 31-45.

[4] Matousek, D. (2014). Comparison of selected architectures of negative Charge Pumps with new design. In *Radioelektronika : 24th International Conference*, April 15-16, 2014. IEEE.

[5] Yamazoe, T., Ishida, H., Nihongi, Y. (2009). A Charge Pump that generates positive and negative high voltages with low power-supply voltage and low power consumption for non-volatile memories. In *International Symposium on Circuits and Systems (ISCAS 2009)*, May 24-27, 2009. IEEE, 988-999.

[6] Wong, O.Y., Wong, R., Tam, W.S., Kok, C.W. (2011). An overview of charge pumping circuits for Flash memory applications. In *9th International Conference on ASIC (ASICON)*, October 25-28, 2011. IEEE, 116-119.

[7] Wong, O.Y., Wong, H., Tam, W.S., Kok, C.W. (2014). On the design of power- and area-efficient Dickson charge pump circuits. *Analog Integrated Circuits and Signal Processing*, 78 (2), 373-389.

[8] Matousek, D., Subrt, O., Hospodka, J. (2015). Charge pump design for use in NVM device test and measurement. In *MEASUREMENT 2015: 10th International Conference*, May 25-28, 2015. Institute of Measurement Science SAS, 203-206.

Received March 29, 2016.
Accepted October 07, 2016.